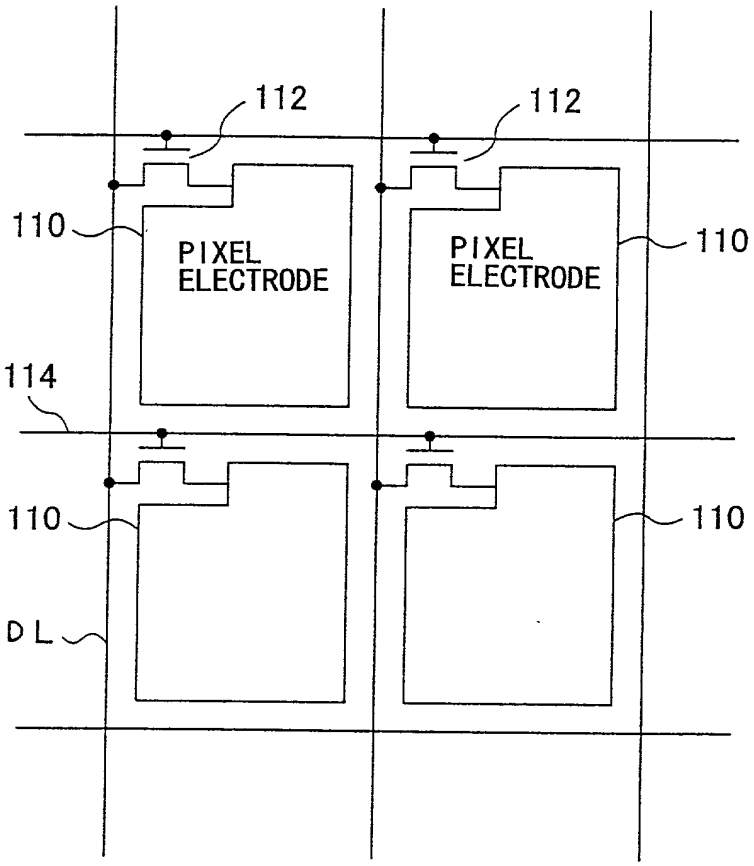
FIG. 1


112
112
110
PIXEL ELECTRODE
PIXEL ELECTRODE
110
114
110
110
DL

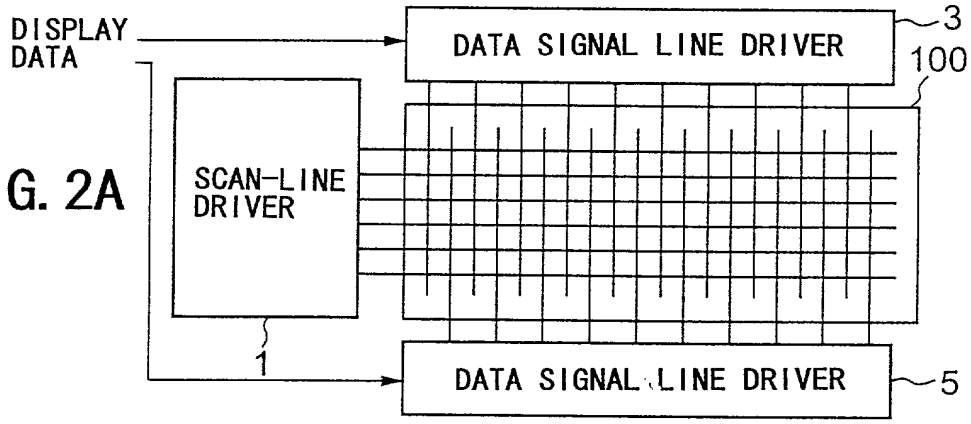

DISPLAY DATA
DATA SIGNAL LINE DRIVER
3
100
SCAN-LINE DRIVER
1
DATA SIGNAL LINE DRIVER
5

FIG. 2A

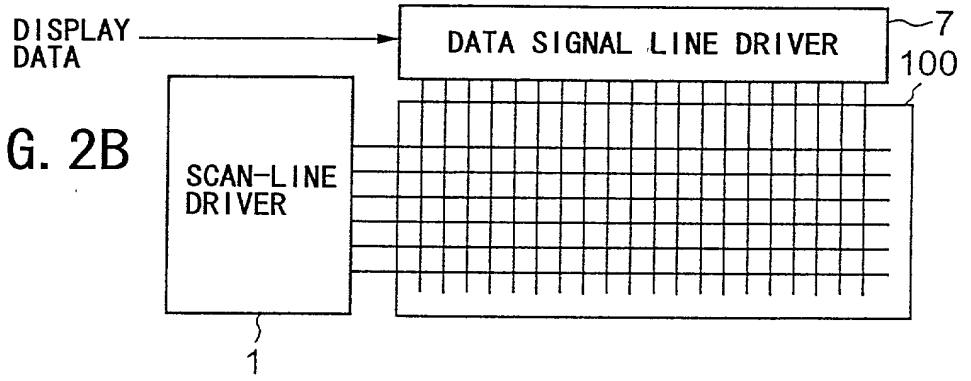

DISPLAY DATA
DATA SIGNAL LINE DRIVER
7
100
SCAN-LINE DRIVER
1

FIG. 2B

FIG.3

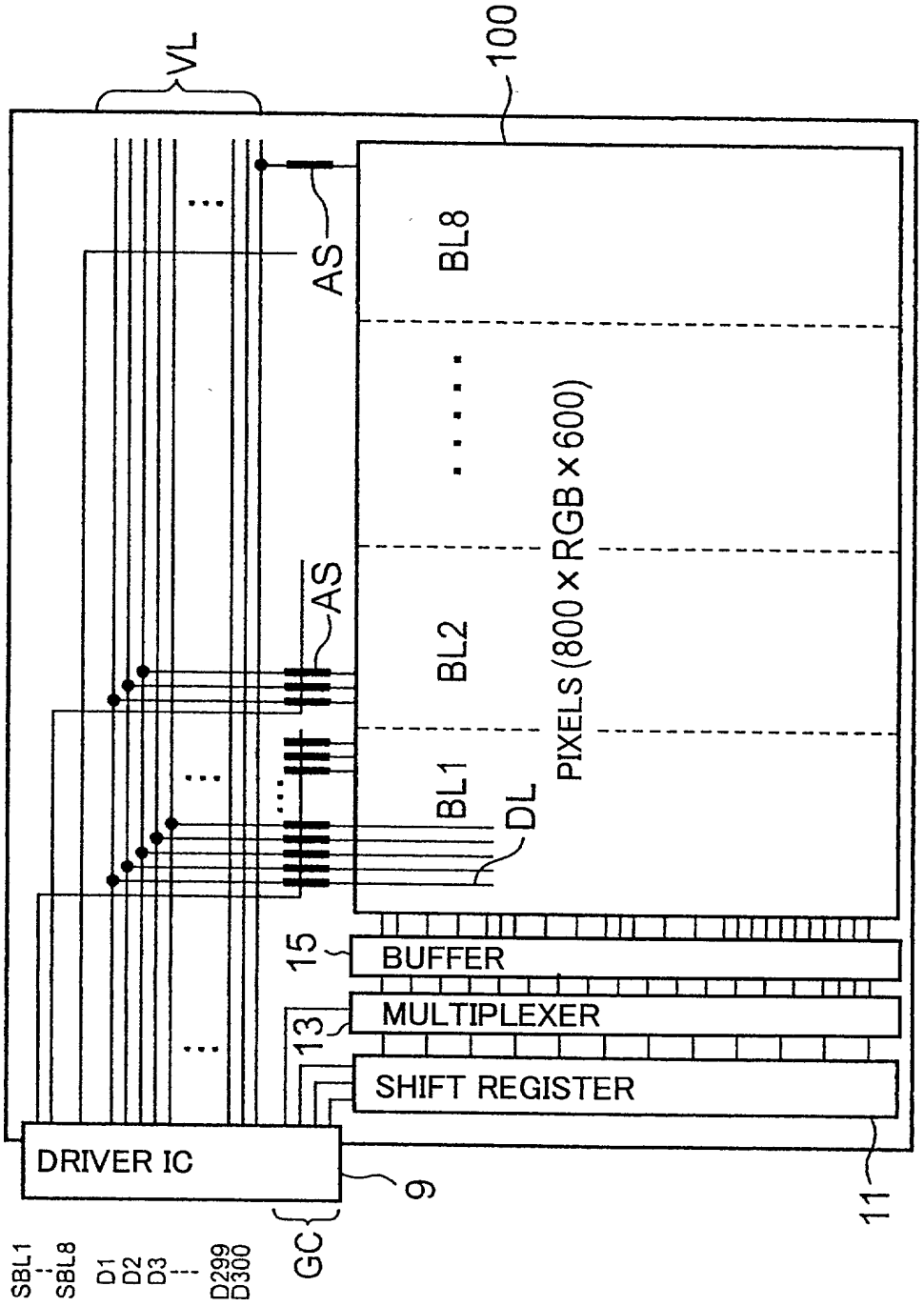

VL
100
AS
BL8
PIXELS (800 × RGB × 600)
BL2
BL1
DL
15
BUFFER
13
MULTIPLEXER
SHIFT REGISTER
DRIVER IC
9
11
SBL1
SBL8
D1
D2
D3
D299
D300
GC

FIG.4

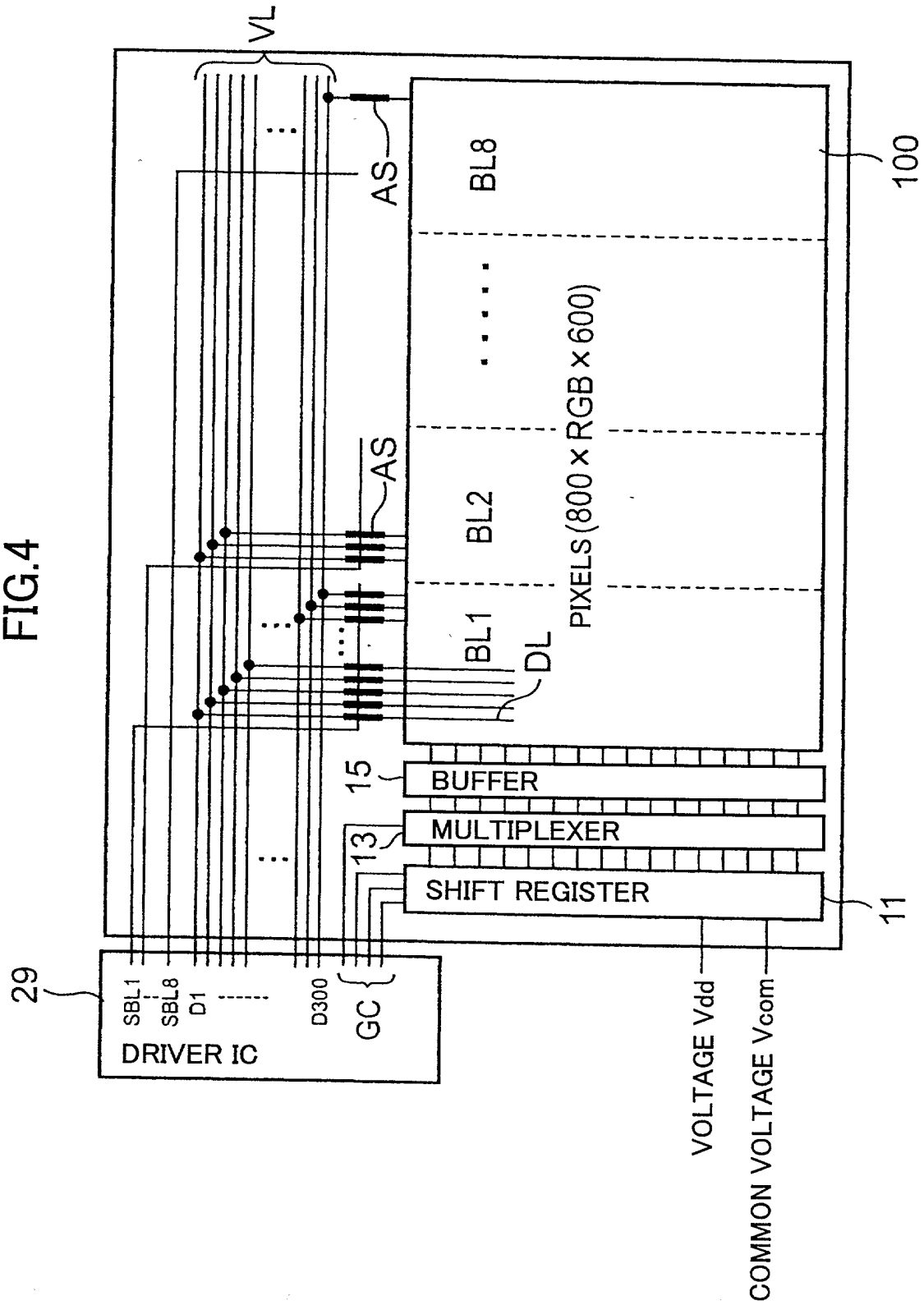
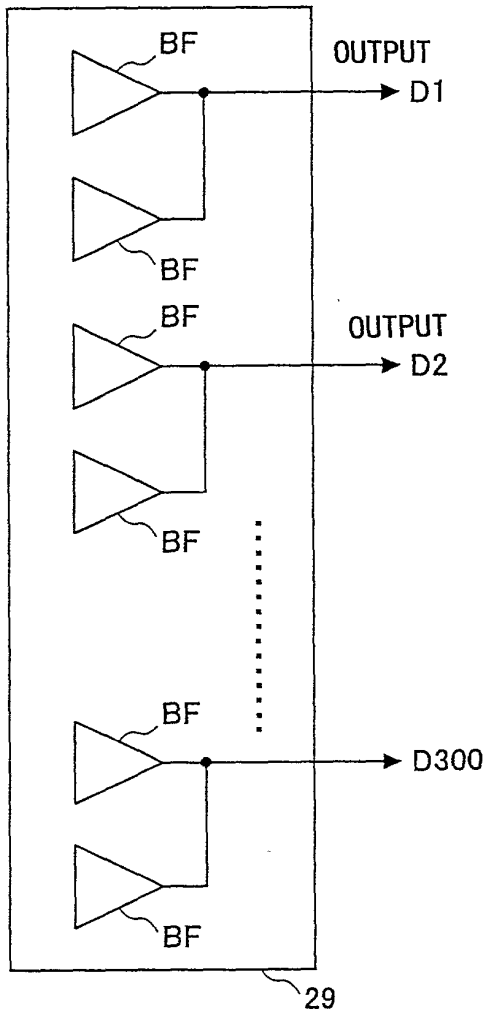

VL
AS
BL8
100
PIXELS (800 × RGB × 600)
BL2
AS
BL1
DL
15
BUFFER
13
MULTIPLEXER
SHIFT REGISTER
11
29
SBL1
SBL8
D1
D300
GC
DRIVER IC
VOLTAGE Vdd
COMMON VOLTAGE Vcom

FIG. 5



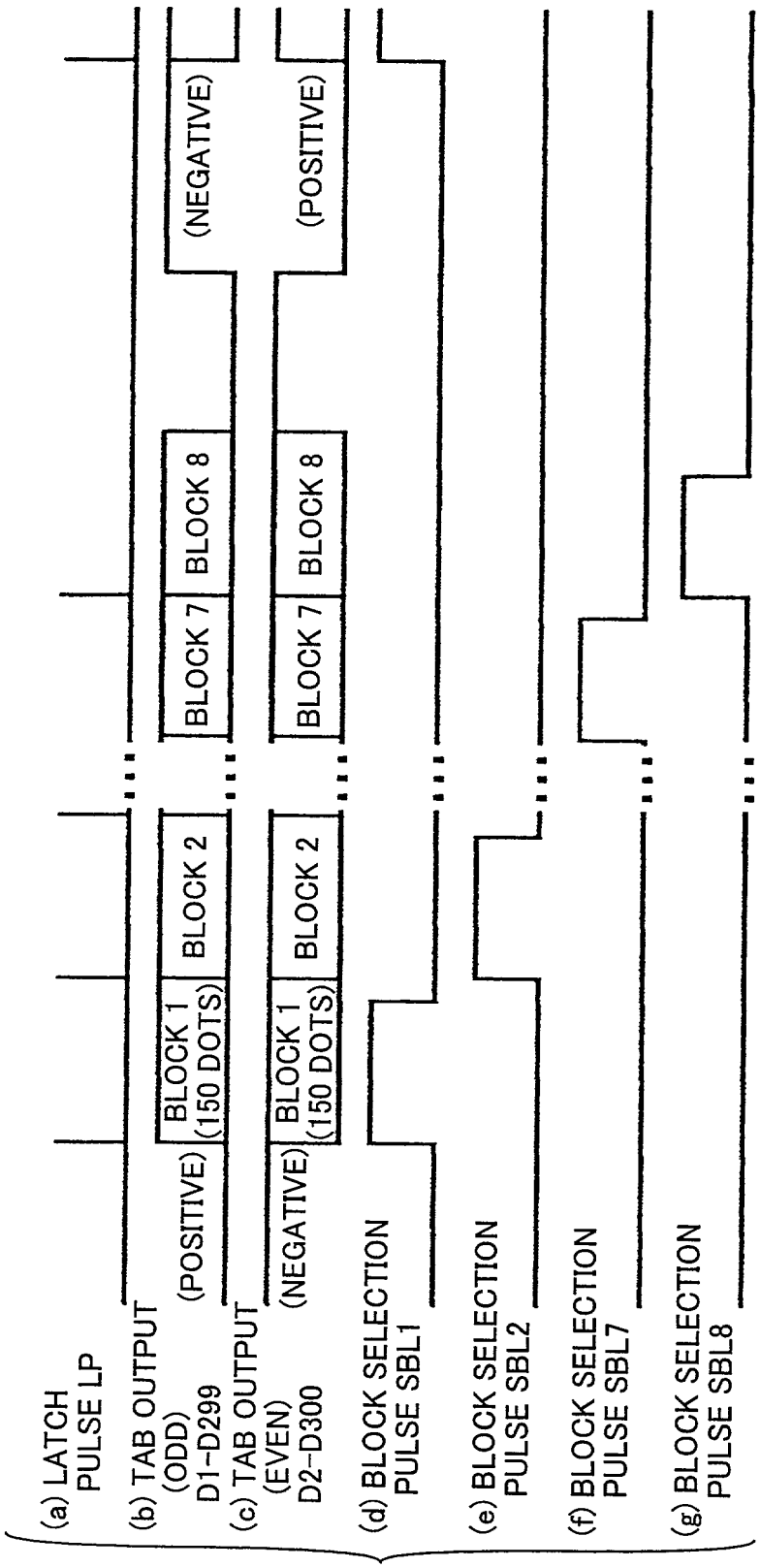

(a) LATCH PULSE LP
(b) TAB OUTPUT (ODD) D1-D299
(POSITIVE)
BLOCK 1 (150 DOTS)
BLOCK 2
BLOCK 7
BLOCK 8
(NEGATIVE)
(c) TAB OUTPUT (EVEN) D2-D300
(NEGATIVE)
BLOCK 1 (150 DOTS)
BLOCK 2
BLOCK 7
BLOCK 8
(POSITIVE)
(d) BLOCK SELECTION PULSE SBL1
(e) BLOCK SELECTION PULSE SBL2
(f) BLOCK SELECTION PULSE SBL7
(g) BLOCK SELECTION PULSE SBL8

FIG.6

FIG.7

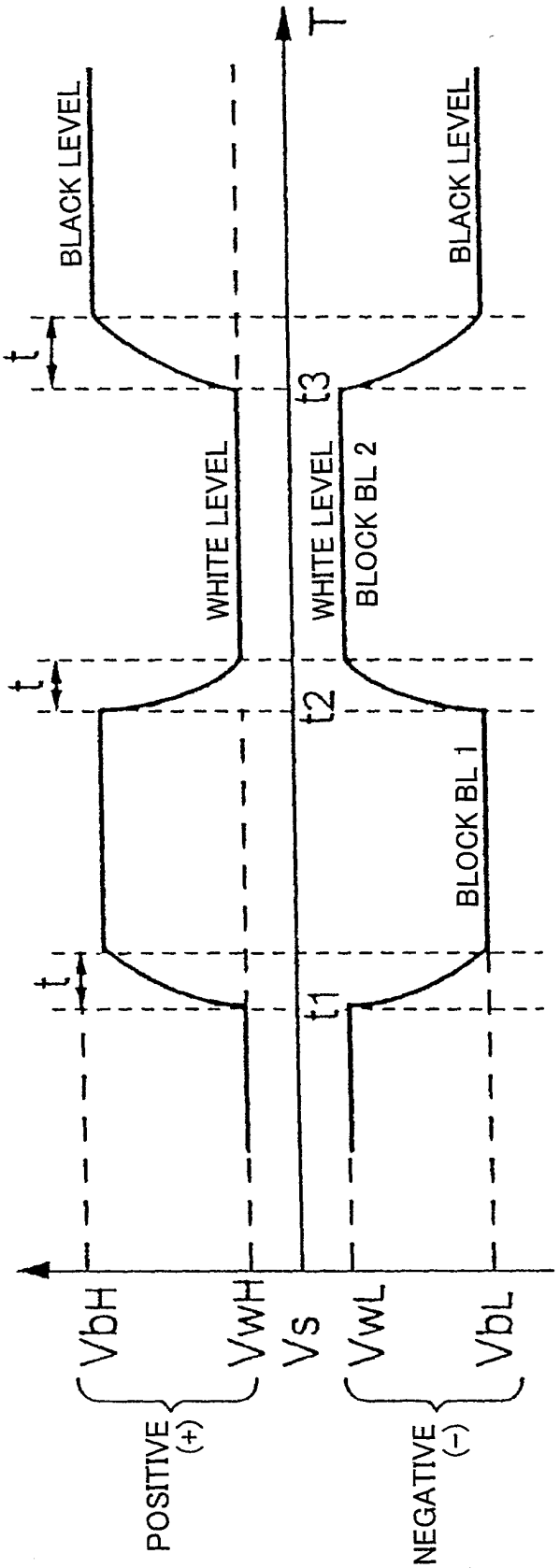

T
BLACK LEVEL
BLACK LEVEL
t
t
t
WHITE LEVEL
WHITE LEVEL
BLOCK BL 2
BLOCK BL 1
t1
t2
t3
VbH
VwH
Vs
VwL
VbL
POSITIVE (+)
NEGATIVE (-)

FIG.8

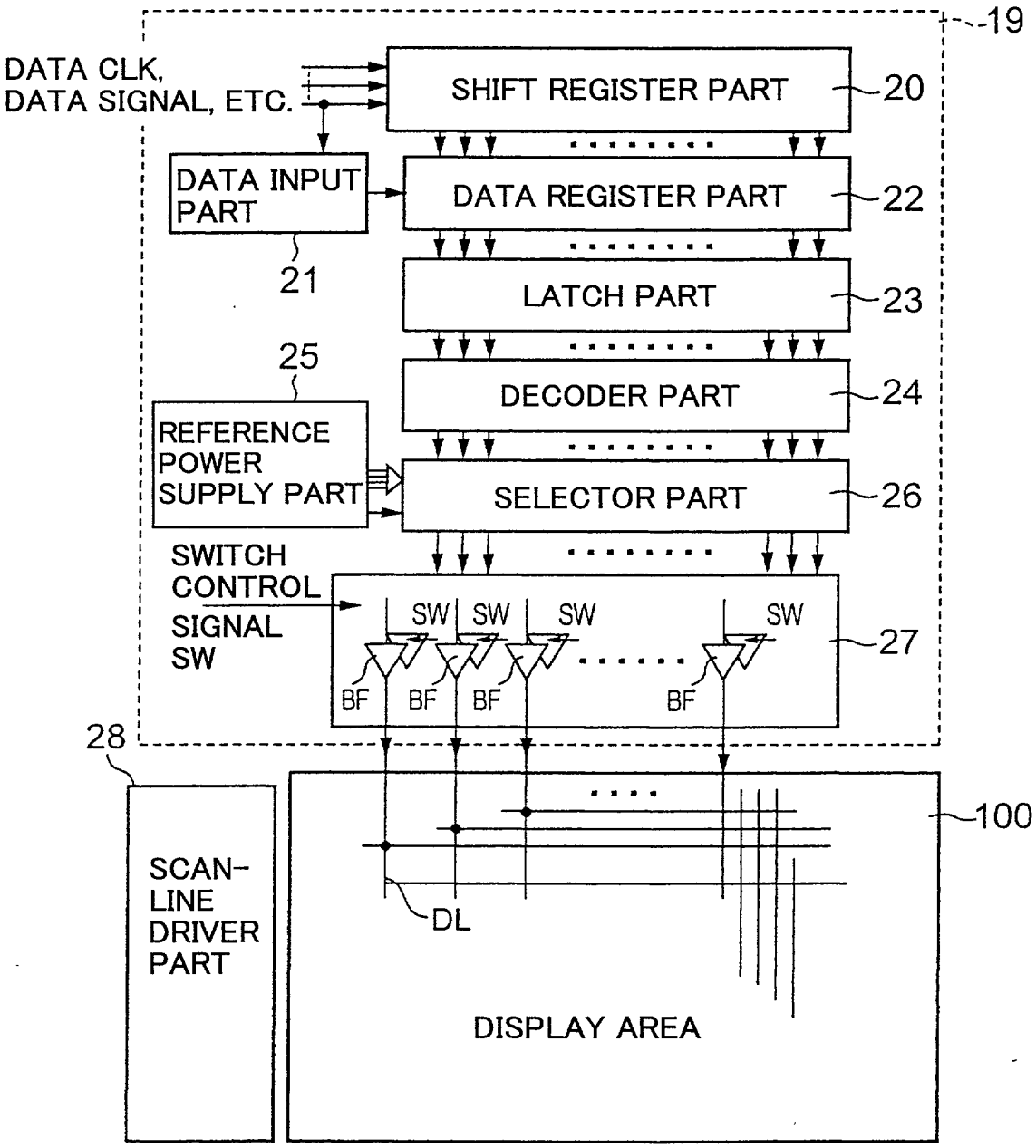

19
DATA CLK,
DATA SIGNAL, ETC.
SHIFT REGISTER PART
20
DATA INPUT PART
DATA REGISTER PART
22
21
LATCH PART
23
25
DECODER PART
24
REFERENCE POWER SUPPLY PART
SELECTOR PART
26
SWITCH CONTROL SIGNAL SW
SW
SW
SW
SW
27
BF
BF
BF
BF
28
100
SCAN-LINE DRIVER PART
DL
DISPLAY AREA

FIG. 9A

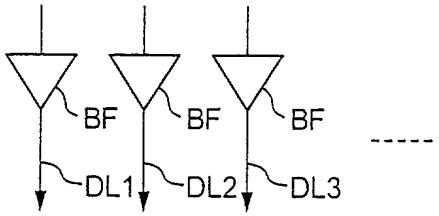


FIG. 9B

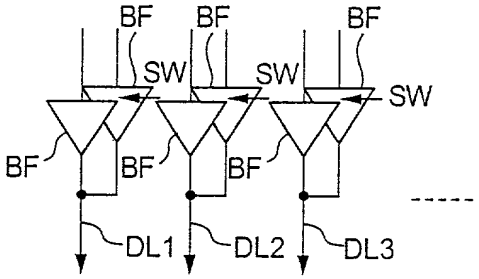


FIG. 9C

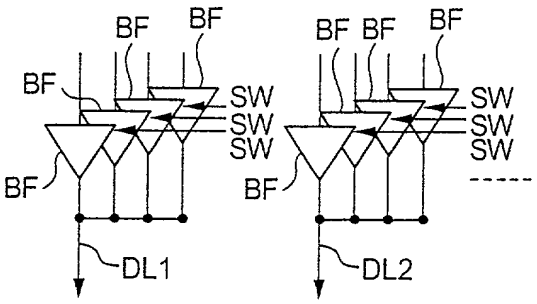


FIG. 10

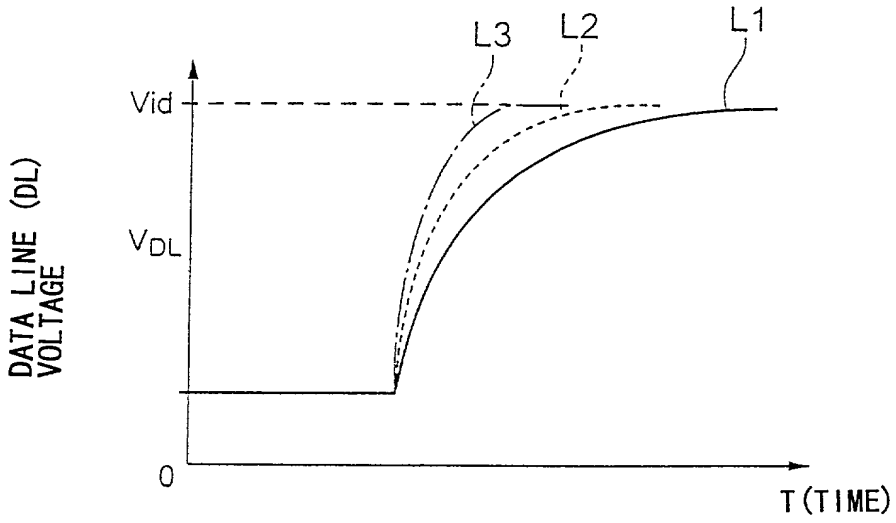


FIG.11

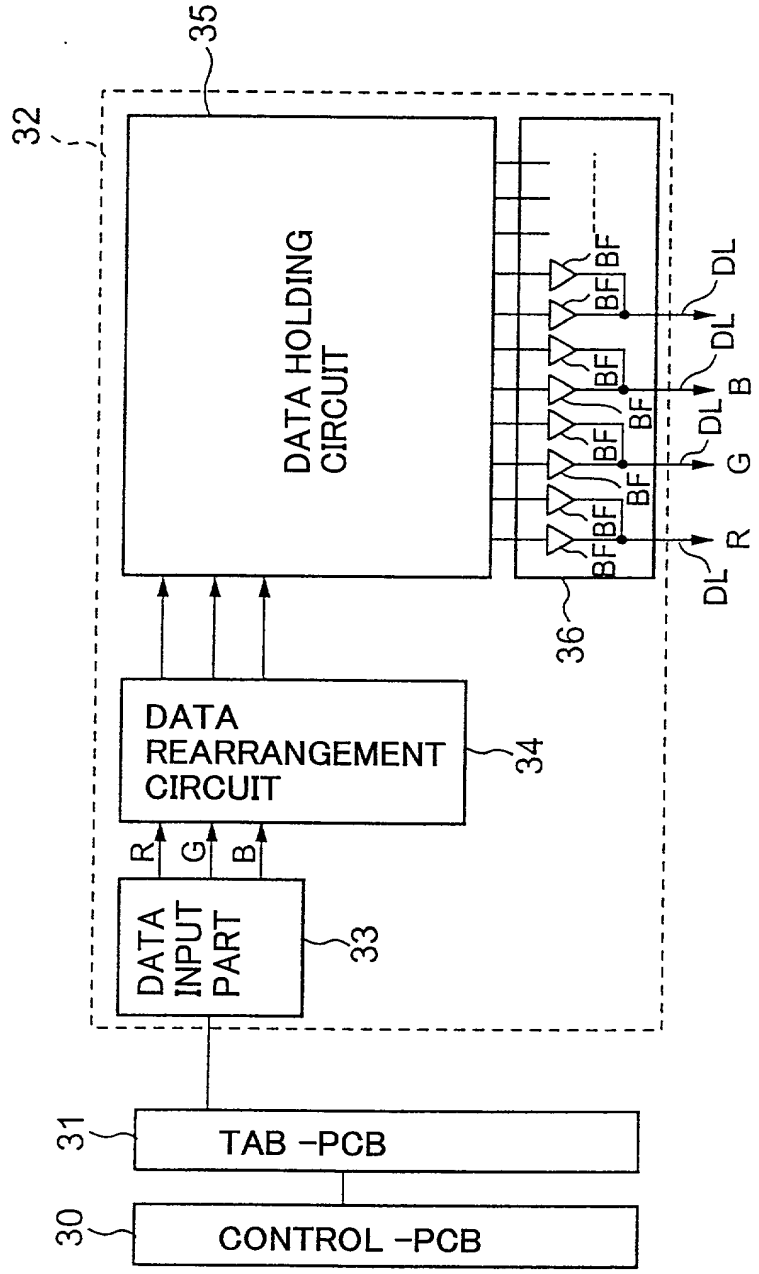

35
32
DATA HOLDING CIRCUIT
BF
DL
R
G
B
36
DATA REARRANGEMENT CIRCUIT
34
R
G
B
DATA INPUT PART
33
31
TAB -PCB
30
CONTROL -PCB

FIG.12

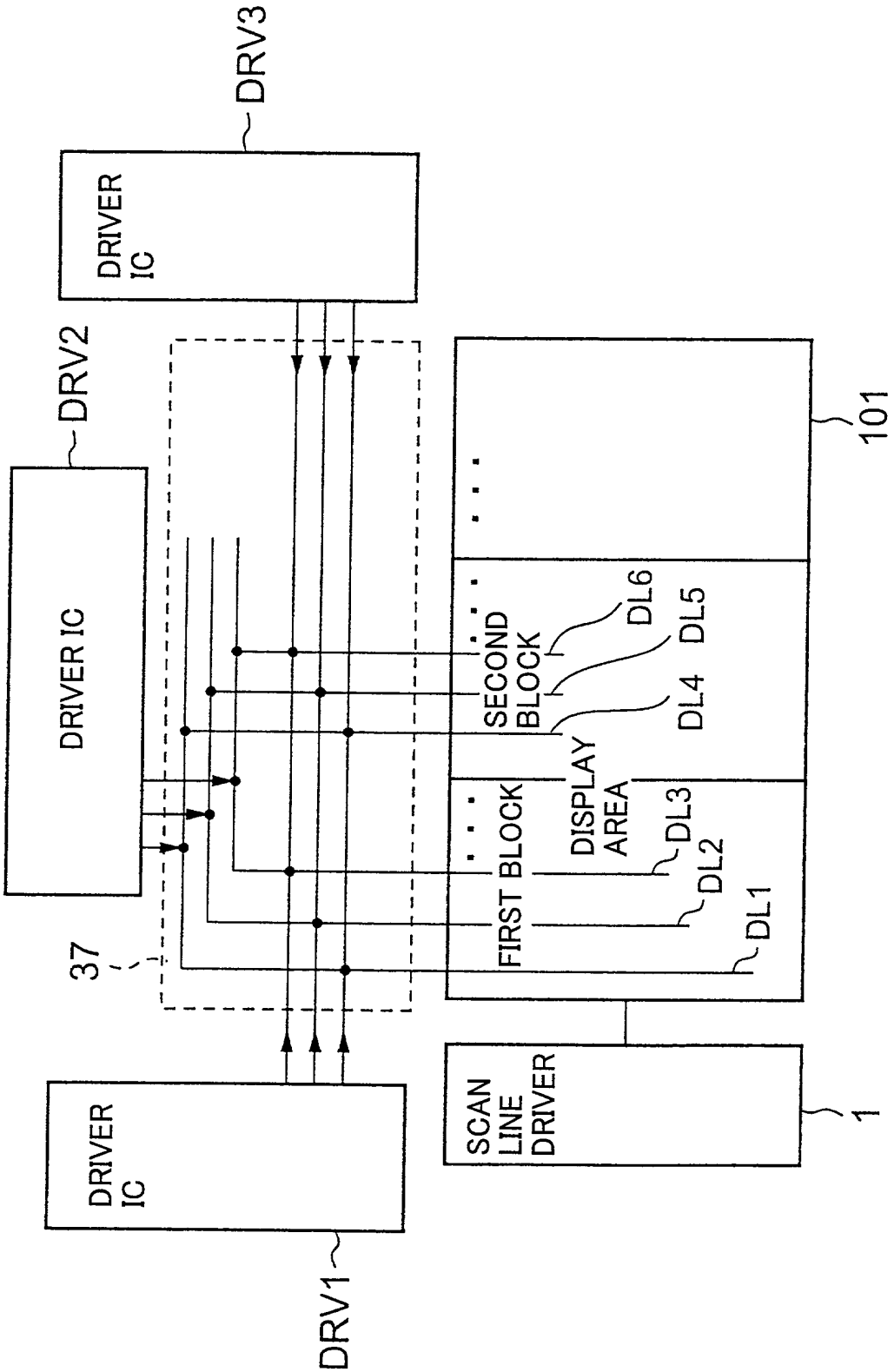

DRV3
DRIVER IC
DRV2
DRIVER IC
37
DRIVER IC
DRV1
101
SECOND BLOCK
FIRST BLOCK
DISPLAY AREA
DL6
DL5
DL4
DL3
DL2
DL1
SCAN LINE DRIVER
1

FIG. 13

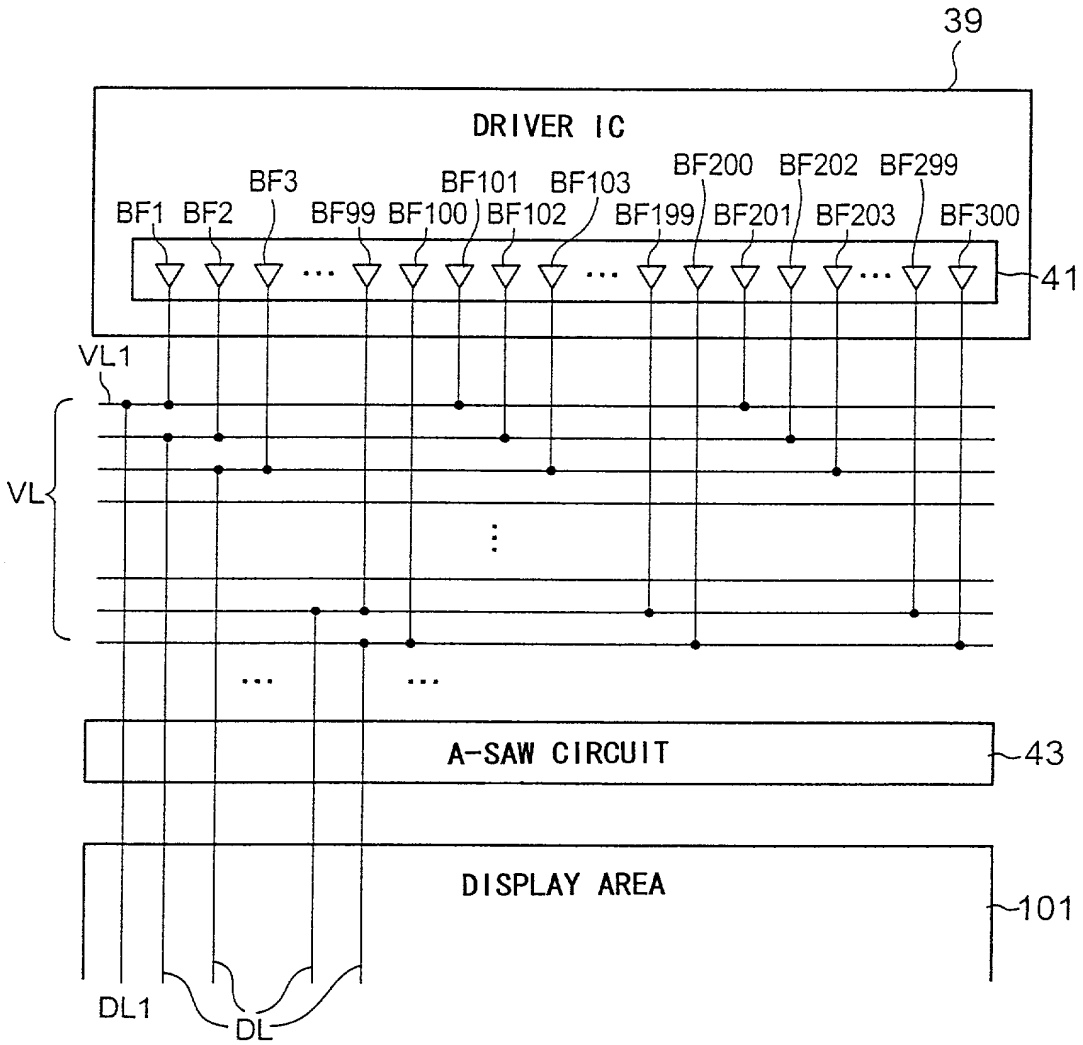

39
DRIVER IC
BF1
BF2
BF3
BF99
BF100
BF101
BF102
BF103
BF199
BF200
BF201
BF202
BF203
BF299
BF300
41
VL1
VL
A-SAW CIRCUIT
43
DISPLAY AREA
101
DL1
DL

FIG.14

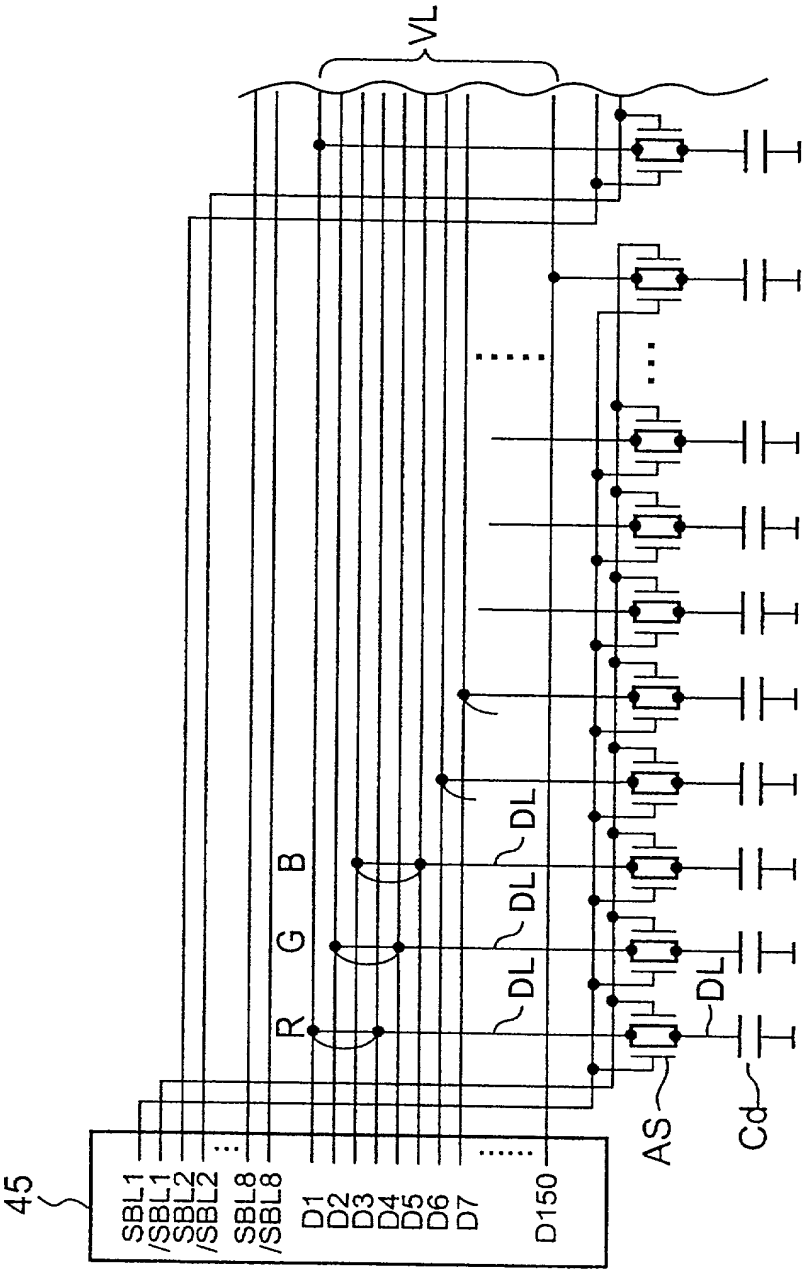

VL
45
SBL1
/SBL1
SBL2
/SBL2
SBL8
/SBL8
R
G
B
D1
D2
D3
D4
D5
D6
D7
D150
DL
AS
Cd

FIG. 15

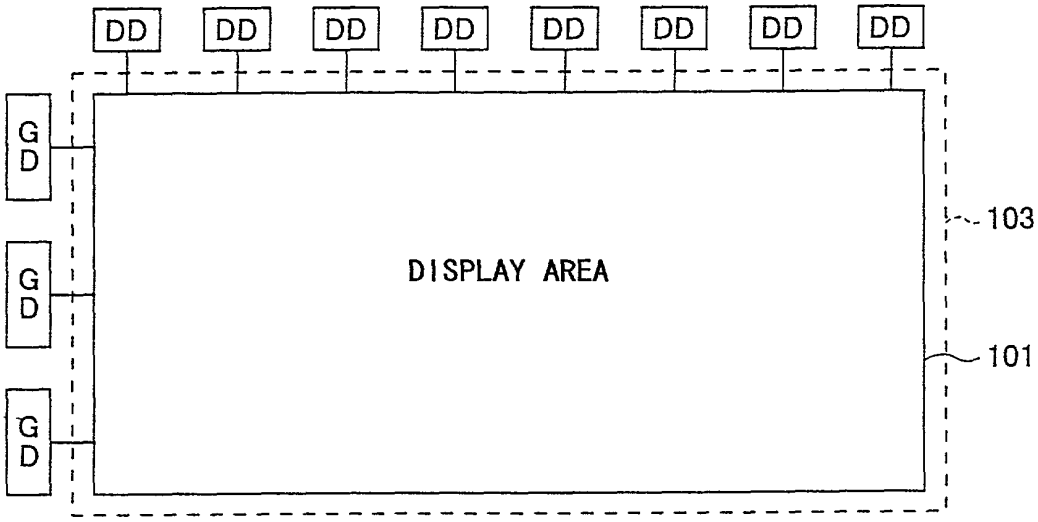


FIG.16

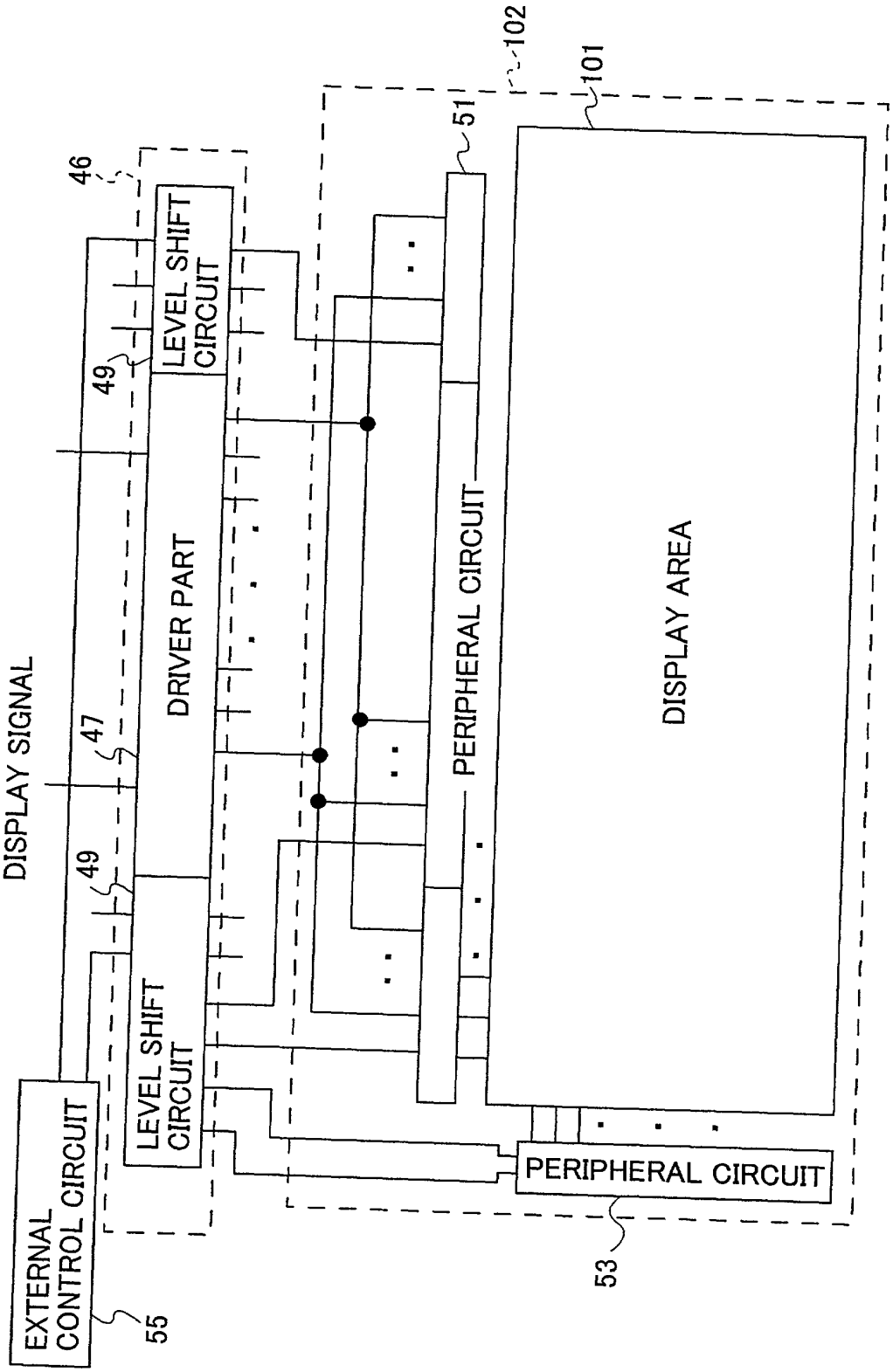

DISPLAY SIGNAL
46
49
LEVEL SHIFT CIRCUIT
47
DRIVER PART
49
LEVEL SHIFT CIRCUIT
EXTERNAL CONTROL CIRCUIT
55
102
101
51
PERIPHERAL CIRCUIT
DISPLAY AREA
PERIPHERAL CIRCUIT
53

FIG.17

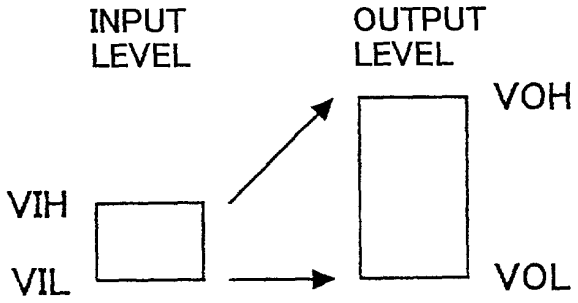
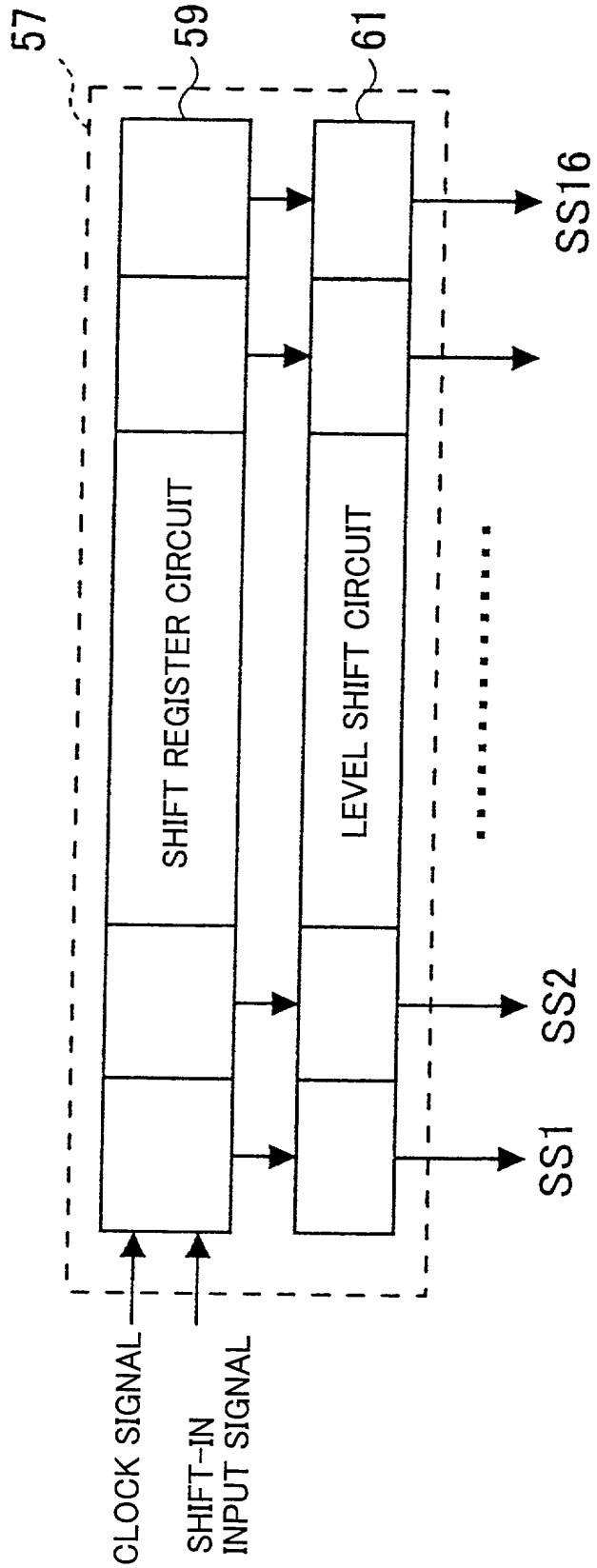


FIG.18


57
59
61
SS16
SHIFT REGISTER CIRCUIT
LEVEL SHIFT CIRCUIT
SS2
SS1
CLOCK SIGNAL
SHIFT-IN INPUT SIGNAL

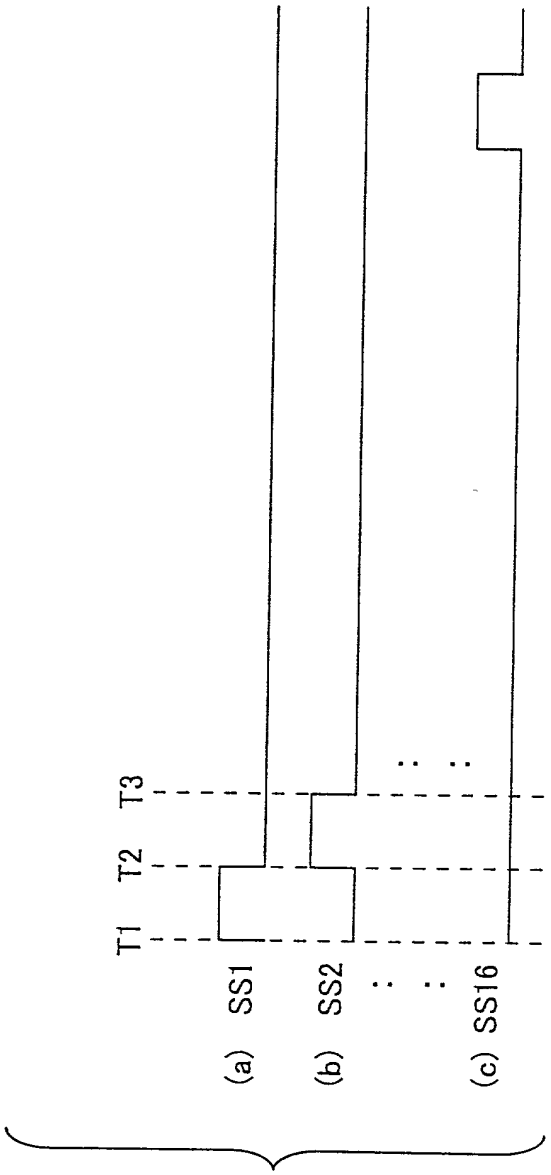


FIG. 19

FIG.20

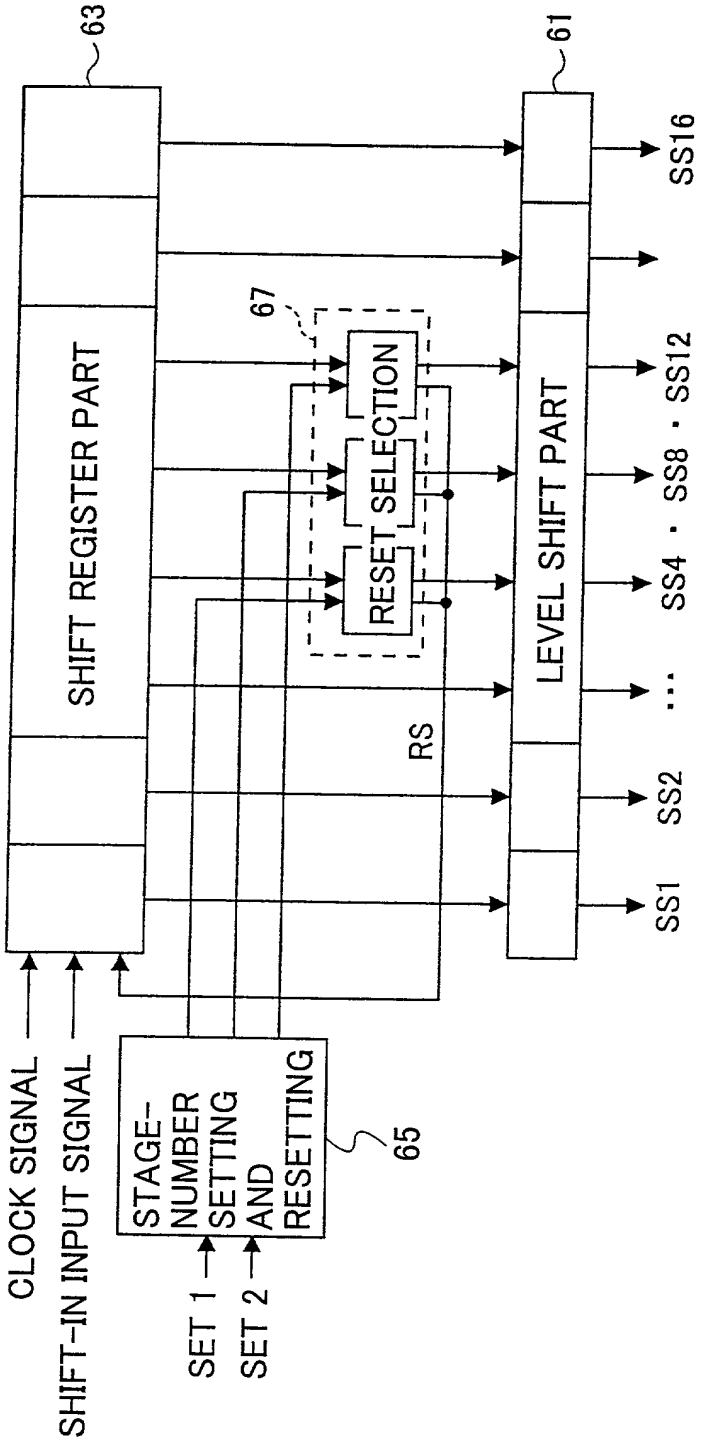

63
61
SHIFT REGISTER PART
LEVEL SHIFT PART
67
RESET SELECTION
RS
CLOCK SIGNAL
SHIFT-IN INPUT SIGNAL
STAGE-NUMBER SETTING AND RESETTING
65
SET 1
SET 2
SS16
SS12
SS8
SS4
SS2
SS1

FIG.21

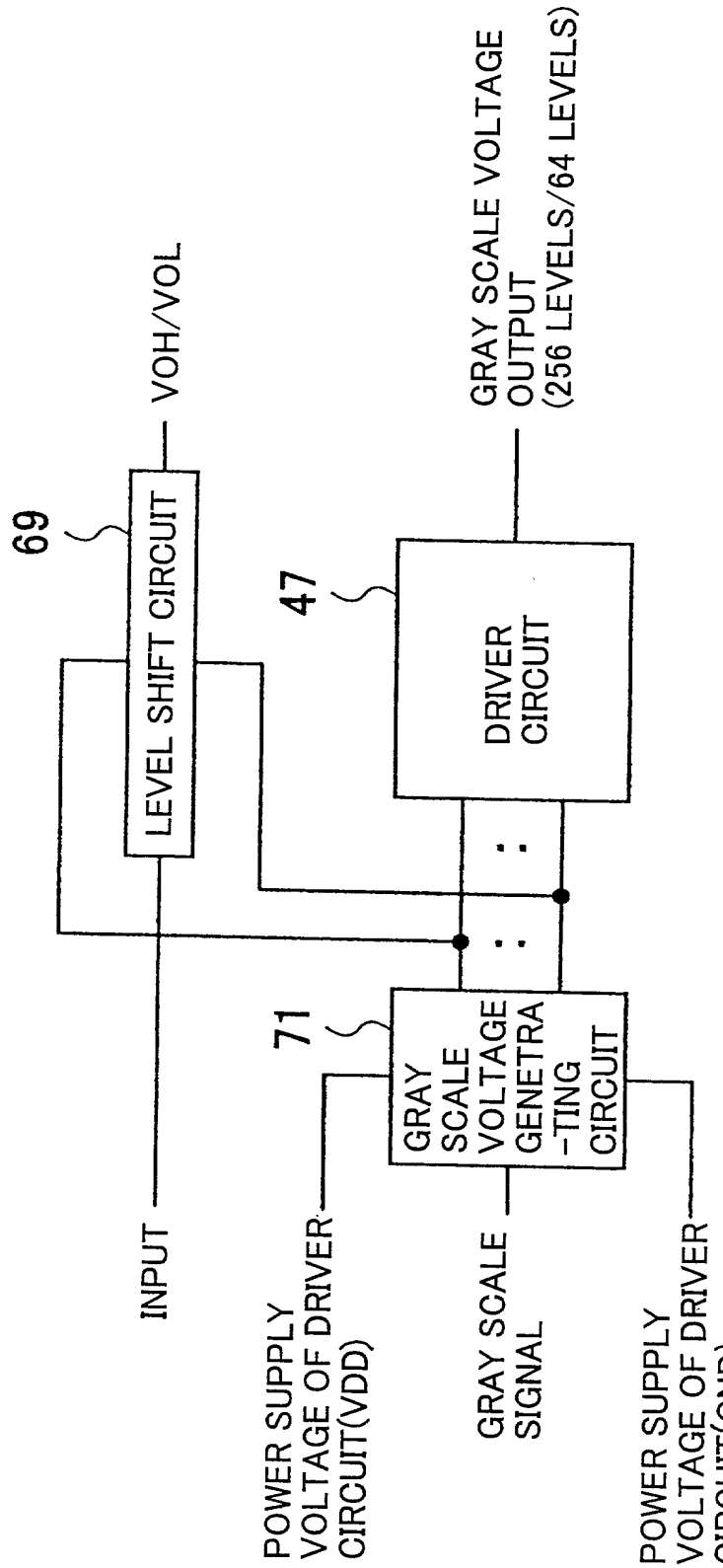
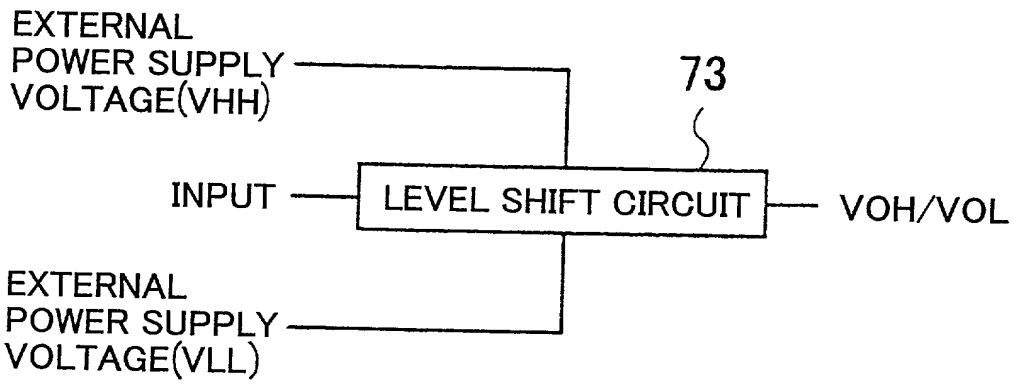

69
LEVEL SHIFT CIRCUIT
VOH/VOL
47
DRIVER CIRCUIT
GRAY SCALE VOLTAGE OUTPUT (256 LEVELS/64 LEVELS)
71
GRAY SCALE VOLTAGE GENETRA -TING CIRCUIT
INPUT
POWER SUPPLY VOLTAGE OF DRIVER CIRCUIT(VDD)
GRAY SCALE SIGNAL
POWER SUPPLY VOLTAGE OF DRIVER CIRCUIT(GND)

FIG.22


EXTERNAL
POWER SUPPLY
VOLTAGE(VHH)
73
INPUT
LEVEL SHIFT CIRCUIT
VOH/VOL
EXTERNAL
POWER SUPPLY
VOLTAGE(VLL)